A NASA Perspective on Validation and Testing of Design Hardening for the Natural Space Radiation Environment

Kenneth A. LaBel
NASA Goddard Space Flight Center, Code 561.4, Greenbelt, MD 20771
1-301-286-9936 / Kenneth.A.Label@nasa.gov

James W. Howard
Jackson & Tull Chartered Engineers, Washington, D. C. 20018
1-301-286-1023 / James.W.Howard.1@gsfc.nasa.gov

Martin A. Carts, and Christina Seidleck
Raytheon Information Technology & Scientific Services, Lanham, MD 20706-4392
1-301-286-2600 and 1-301-286-1009 / Martin.A.Carts.1@gsfc.nasa.gov and Christina.M.Seidleck.1@gsfc.nasa.gov

Abstract

With the dearth of dedicated radiation hardened foundries, new and novel techniques are being developed for hardening designs using non-dedicated foundry services. In this paper, we will discuss the implications of validating these methods for the natural space radiation environment issues: total ionizing dose (TID) and single event effects (SEE). Topics of discussion include:

- *Types of tests that are required,*
- *Design coverage (i.e., design libraries: do they need validating for each application?), and*
- *A new task within NASA to compare existing design hardening techniques.*

This latter task is a new effort in FY03 utilizing a 8051 microcontroller core from multiple design hardening developers as a test vehicle to evaluate each mitigative technique.

1. INTRODUCTION

NASA constantly strives to provide the best capture of science while operating in a space radiation environment using a minimum of resources [1]. With a relatively limited selection of radiation-hardened microelectronic devices (a handful of foundry options) that are often two or more generations of performance behind commercial state-of-the-art technologies, NASA's performance of this task is quite challenging. One method of alleviating this dichotomy (a radiation-tolerance need and higher electrical performance) is by the use of commercial foundry alternatives with no or minimally-invasive design techniques for hardening. This is often called hardened-by-design (HBD, as opposed to the traditional hardened-by-process associated with radiation hardened devices). Building custom-type HBD devices using design libraries and automated design tools may provide NASA the solution it needs to meet stringent science performance specifications in a timely, cost-effective, and reliable manner.

However, one question still exists: traditional radiation-hardened devices have lot and/or wafer radiation qualification tests performed; what types of tests are required for HBD validation?

2. Radiation Effects Considerations

From the NASA engineering perspective, the natural space environment is the enemy for our space systems. Ionizing radiation effects on complementary metal oxide semiconductor (CMOS) electronics can be separated into two areas: total ionizing dose (TID) and single event effects (SEE) [2]. The two effects are distinct, as are the testing requirements and HBD techniques considered.

TID is due to long-term degradation of electronics due to the cumulative energy deposited in a material. Effects include parametric failures, or variations in device parameters such as leakage current, threshold voltage, etc., and functional failures.

Significant sources of TID exposure in the space environment include trapped electrons, trapped protons, and solar protons. Ground irradiation typically relies on Co-60, X-ray, electron, or proton sources.

SEEs occur when a single ion strikes the material, depositing sufficient energy in the device to cause an SEE. The many types of SEE may be divided into two main categories: soft errors and hard errors. In general, a soft error occurs when a transient pulse or bit-flip in the device causes an error detectable at the device output. Therefore, soft errors are entirely device specific, and are best categorized by their impact on the device. Single Event Upset (SEU) is generally a transient pulse or bit-flip. In combinatorial logic or an analog-to-digital converter, a transient or spike (single event transient or SET) on the device output would be a potential SEU; in a memory cell or latch, a bit-flip would be an SEU. SEUs occurring in the device's control circuitry may also cause other effects. In general, SEUs are corrected by resetting the device or rewriting the data. During a SEU to a control or test portion of a device (a Single Event Functional Interrupt (SEFI)), the device halts normal operations, and can require a power reset to recover.

Hard errors may be - but are not necessarily - physically destructive to the device, and cause permanent functional effects. Single Hard Error (SHE) causes a permanent change to the operation of the device. A common example would be a stuck bit in a memory device. Single Event Latchup (SEL) is a potentially destructive condition involving parasitic circuit elements. During a traditional or destructive SEL, the device current exceeds the maximum specified for the device. Unless power is removed, the

device will eventually be destroyed. A micro-latch is a type of SEL where the device current is elevated, but below the device's specified maximum. Again, a power reset is required to recover normal device operation. Single Event Burnout (SEB) is a highly localized destructive burnout of the drain-source in power MOSFETs (metal oxide semiconductor field effect transistors). Single Event Gate Rupture (SEGR) is the destructive burnout of a gate insulator in a power MOSFET. One should note that even current limiting solutions may not mitigate the problem; a latent damage mechanism can be present that can cause a later device failure.

The SEE sensitivity of a device is discussed in terms of Linear Energy Transfer (LET) and Cross Section (σ). LET is a measure of the energy deposited per unit length as an ionizing particle travels through a material. The common unit is MeV*cm^2/mg of material (Si for MOS devices). LET threshold (LET_{th}) is the minimum LET to cause an effect, at a given particle fluence of 1E6 or 1E7 ions/cm^2. The σ reflects the device area which is sensitive to ionizing radiation. For a specific LET, cross section is calculated: σ = #errors/particle fluence. The units for cross section are cm^2 per device or per bit. Sensitive volume refers to the device volume affected by SEE-inducing radiation. The sensitive volume is, in general, much smaller than the actual device volume.

Significant sources of SEE exposure in the space environment include galactic cosmic rays (GCRs), trapped protons, and solar protons. Ground-based SEE tests involve heavy ion accelerators or proton facilities. Other tools such as laser-irradiation are used in conjunction.

3. Testing HBD Devices: Test Considerations

Test methodologies in the United States exist to qualify individual devices through standards and organizations such as ASTM, JEDEC, and MIL-STD-1019. Typically, TID (Co-60) and SEE (heavy ion and/or proton) are required for device validation. So what is unique to HBD devices?

As opposed to a "regular" commercial-off-the-shelf (COTS) device or application specific integrated circuit (ASIC) where no hardening has been performed, one needs to determine how validated the design library is as opposed to determining the device hardness. That is, by using test chips can we "qualify" a future device using the same library? Let's discuss an imaginary scenario and some associated test considerations.

Vendor A has designed a new HBD library portable to foundries B and C. A test chip is designed, tested, and deemed acceptable. Nine months later a NASA flight project enters the mix by designing a new device using Vendor A's library. Does this device require complete radiation qualification testing? Maybe...

The first consideration would be: does the HBD technique cover both TID and SEE effects or does it rely on some inherent radiation properties at Vendor B and C's foundries? If for example, Vendor B and C were chosen for inherent SEL hardness (while the HBD covers other SEE and TID) any process change might then require a new qualification test be performed. One could simply select Vendor C's process if B's has changed. Exchanging TID for SEL could provide a similar scenario.

How complete was the test chip? Was there sufficient statistical coverage of all library elements to validate each cell? If the new NASA design uses a partially or insufficiently characterized portion of the design library, full testing might be required. Of course if part of the HBD was relying on inherent radiation hardness of a process, some of the tests (like SEL in the earlier example) may be waived.

Other considerations include speed of operation and operating voltage. For example, if the test chip was tested statically for SEE at a power supply voltage of 3.3V, is the data applicable to a 100 MHz operating frequency at 2.5? Dynamic considerations (i.e., non-static operation) include the propagated effects of SETs. These can be a greater concern at higher frequencies.

The reader should get the gist of the considerations at this point:

- know the design library,
- know the library coverage during testing,
- know the application (speed, voltage, etc.), and
- know the foundry.

If all the above are applicable or have been validated by the test chip, then no testing may be necessary. A new task within NASA's Electronic Parts and Packaging (NEPP) Program is exploring these types of considerations.

4. HBD Technology Evaluation Using the 8051 Processor

With their increasing capabilities and lower power consumption, microcontrollers are increasingly being used in NASA and DOD system designs. There are existing NASA and DoD programs that are doing technology development to provide HBD. Microcontrollers are one such vehicle that is being investigated by both NASA and DoD to quantify the radiation hardness improvement. Examples of these programs are the 8051 microcontroller being developed by Mission Research Corporation (MRC) and the NASA Institute of Advanced Microelectronics (NIAM). As these HBD technologies become available, validation of the technology, in the natural space radiation environment, for NASA's use in spaceflight systems is required.

The 8051 microcontroller is an industry standard architecture that has broad acceptance, wide-ranging applications and development tools available. There are numerous commercial vendors that supply this controller or have it integrated into some type of system-on-a-chip structure. Both MRC and NIAM chose this device to demonstrate two distinctly different technologies for hardening. The MRC example of this is to use temporal latches that require specific timing to ensure that single event effects are minimized. The NIAM technology uses ultra low power and layout and architecture design rules to achieve their results. These are fundamentally different than the approach by Aeroflex-United Technologies Microelectronics Center (UTMC), the commercial vendor of a radiation-hardened 8051, that built their 8051 microcontroller using radiation hardened processes. This broad range of technology within one device structure makes the 8051 an ideal vehicle for performing this technology evaluation.

The advantage that both MRC and NIAM have over UTMC is the portability of the design principles to other device structures. This could possible allow for radiation hardened devices that are much faster to development and thereby much lower cost. The

disadvantage, at this point, is that they are not evaluated technologies for broad use in NASA missions. Without this technology evaluation, approving device usages made with this these technologies would have to be done on a part-by-part, and usage-by-usage basis – leading to large costs.

The objective of this work is the technology evaluation of two technology development areas. The CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) process from the NIAM and the Hardened-by-Design process from MRC will be tested for radiation tolerance and reliability. These two processes will be baselined against two other processes, a completely commercial process and a radiation hardened process. By performing this side-by-side comparison allows for the cost benefit, performance and reliability trade study to be done (i.e., the high cost of radiation hardened process versus the cost and performance benefit of the commercial process versus the two technology development processes).

In the performance of the technology evaluation, this task will be developing test structures and software for testing microcontrollers. A thorough process will be done in this task to optimize the test process to obtain as complete an evaluation as possible. This will include taking advantage of any hardware available and writing software that exercises the microcontroller is such a manner to evaluate substructures of the processor. This process will lead to a more complete understanding of how to test complex structures, such as microcontrollers, and how to more efficiently test these structures in the future.

For the hardware side, the 8051 Device Under Test (DUT) will be tested as a component of a functional computer as illustrated in Figure 1. Aside from DUT itself, the other components of the DUT computer will be removed from the immediate area of the irradiation beam. A small card (one per DUT package type) with a unique hard-wired identifier byte will contain the DUT, its crystal, and bypass capacitors. This "DUT Board" will be connected to the "Main Board" by a short 60-conductor ribbon cable. The Main Board will have all other components required to complete the DUT Computer, including some which nominally are not necessary in some designs (such as external RAM, external ROM and address latch).

The DUT Computer boots by executing the instruction code located at address 0x0000. Initially, the device at this location will be an EPROM previously loaded with "Boot/Serial Loader" code. This code will initialize the DUT Computer and interface through a serial connection to the controlling computer, the "Test Controller". The DUT Computer will download Test Code and put it into Program Code RAM (located on the Main Board of the DUT Computer). It will then activate a circuit which will simultaneously perform two functions: Hold the DUT reset line active for some time (perhaps 10 ms); and remap the Test Code residing in the Program Code RAM to locate it to address 0x0000 (the EPROM will no longer be accessible in the DUT Computer's memory space). Upon awaking from the reset, the DUT computer will again boot by executing the instruction code at address 0x0000, except that this time that code will not be the Boot/Serial Loader code but the Test Code.

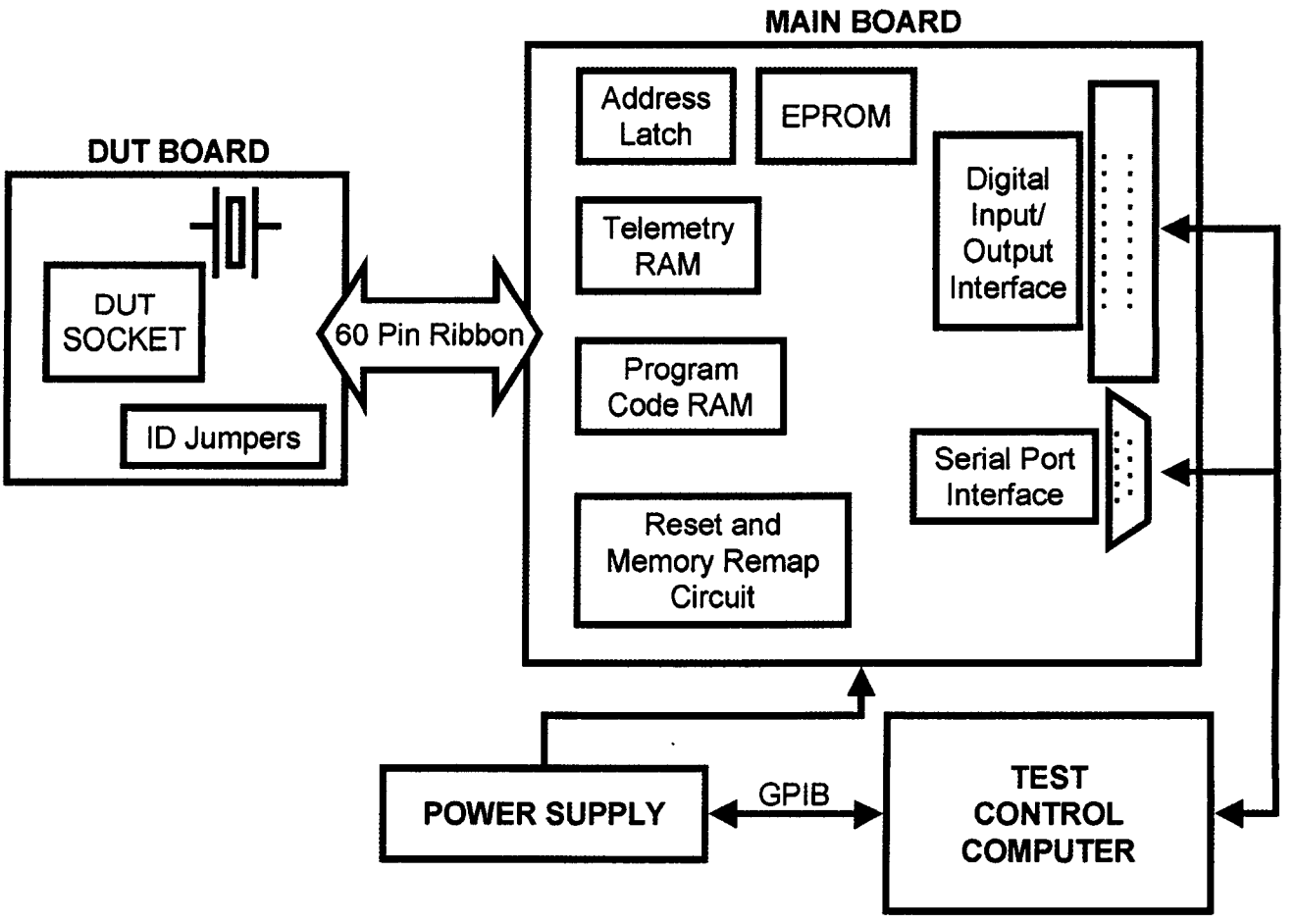

Figure 1. Hardware Block Diagram of the Test System.

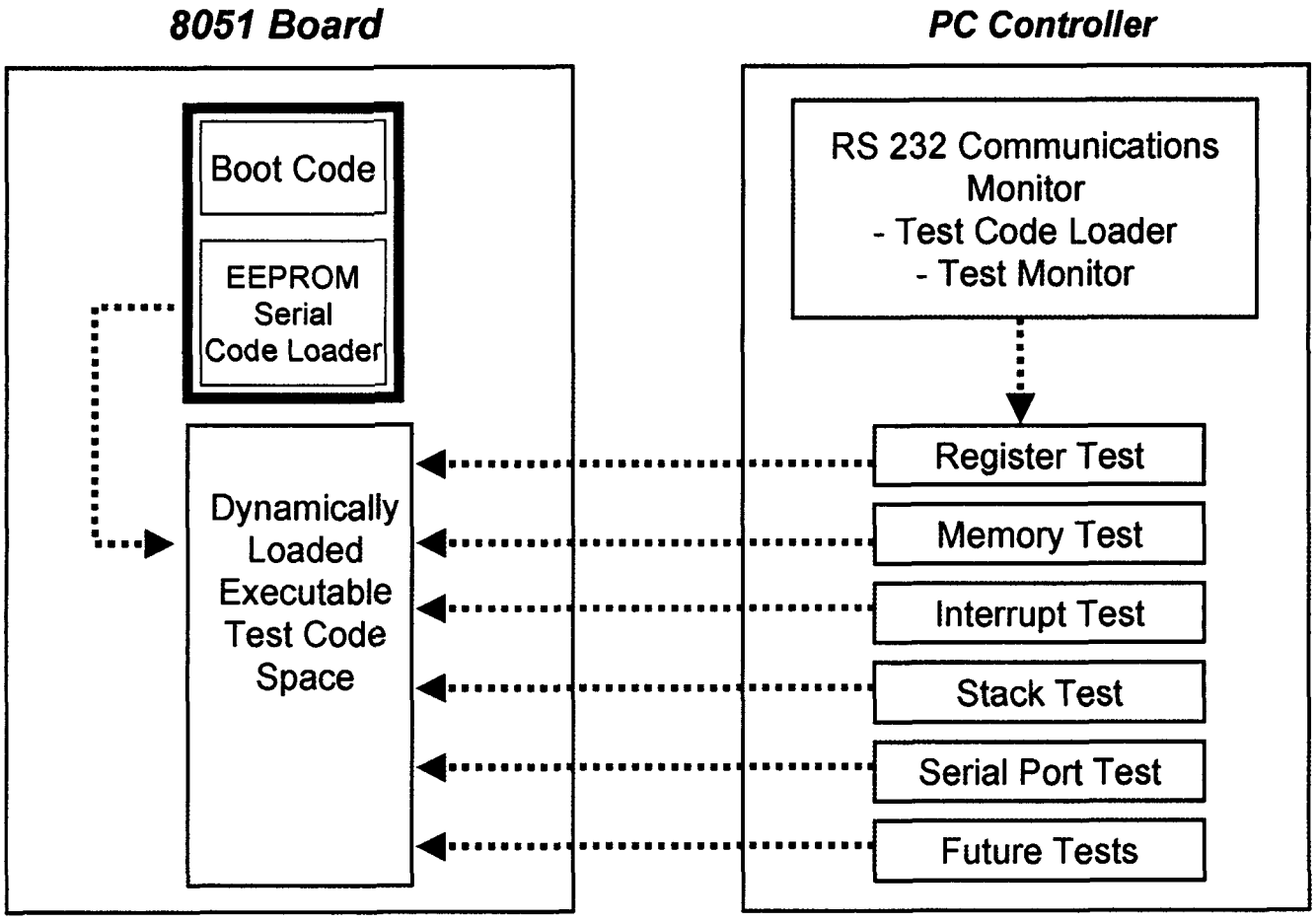

Figure 2. Test Software Block Diagram.

The Test Controller always retains the ability to force the reset/remap function, regardless of the DUT Computer's functionality. Thus, if the test progresses without crash (Single Event Functional Interrupt, SEFI) either the DUT Computer itself or the Test Controller can terminate the test and allow the post-test functions to be executed. If a SEFI occurs, the Test Controller will force a reboot into Boot/Serial Loader code and will then execute the post-test functions.

During any test of the DUT, the DUT will exercise a portion of its functionality (e.g. Register operations or Internal RAM check, or Timer operations) at the highest utilization possible, while making a minimal periodic report to the Test Controller to convey that the DUT Computer is still functional. Should this report cease the Test Controller will know that a SEFI has occurred. This periodic data is called "telemetry". If the DUT encounters an error that is not interrupting the functionality (e.g., a data register miscompare) it will send a more lengthy report through the serial port describing that error, and then will continue with the test.

The 8051 test software concept is fairly straightforward. It is designed to be a modular series of small test programs each with a specific part of the DUT to exercise (Figure 2). Since each test is stand alone, they can be loaded independently of each other for execution on the DUT. This ensures that only the desired portion of the 8051 DUT is being exercised during the test and will help pinpoint location of errors that occur during testing. All test programs will reside on the controller PC until loaded via the serial interface to the DUT computer. In this way, individual tests may be modified (possibly for adaptation to a different 8051 device) at any time without the necessity of burning PROMs. Additional tests may be developed and added as needed without impacting the overall test design. The only permanent code, which will be resident on the DUT, will be boot code and serial code loader routines that will establish communications between the controller PC and the DUT.

5. Final Considerations

Like any new research effort, one can expect some unexpected "features" along the way. Changes in standard tool platforms, advent of reprogrammable devices, etc. will bring new fruit to bear on the HBD approaches. Validation must be treated thoughtfully and carefully with knowledge of the process and the limitations of the HBD techniques being key.

The bottom line is that some new designs may require further or complete tests while others may require none or a limited few.

6. ACKNOWLEDGEMENTS

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7. References

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8. BIBLIOGRAPHY (IES)

Kenneth A. LaBel graduated from the Johns Hopkins University in 1983 with a BES in Electrical Engineering and Computer Science with a minor in Mathematical Sciences. Since his graduation, Mr. LaBel has worked at NASA's Goddard Space Flight Center (GSFC). In this time period, he has worked many differing areas. They include:

- Ground Systems Engineering
- Robotics Control Systems Design
- Advanced Fiber Optic Network Development
- Command and Data Handling Systems Engineering
- Radiation Effects and Analysis

Mr. LaBel first began radiation effects work in 1990 and has led the Radiation Effects and Analysis group at GSFC ever since. His technology specialties include COTS electronics, fiber optics, and processors, and has championed radiation engineering as a systems level discipline. In addition, he has been Principal Investigator on multiple flight experiments. He currently is Project Manager for the radiation project under the NASA Electronic Parts and Packaging (NEPP) Program and Experiments Manager for the Living With a Star (LWS) Space Environment Testbed (SET).

James W. Howard Jr. manages the Radiation Engineering Group with Jackson & Tull Chartered Engineers. Dr. Howard received a BS in Nuclear Engineering from Rensselaer Polytechnic Institute (RPI) in 1980 and was commissioned in the US Navy. He also completed graduate work with an MS in both Nuclear Engineering and Mathematics in 1987 and a PhD in Nuclear Engineering and Science in 1990, all from RPI. Since then he has worked as a Research Professor and Associate Director of the Gaerttner LINAC Laboratory at RPI, an on-site contractor at the NASA Marshall Space Flight Center, and finally as an on-site contractor at the Goddard Space Flight Center in the Radiation Effects and Analysis Group. Dr. Howard is very active in the IEEE and has authored or co-authored numerous papers on the effects of radiation on electronics. His current efforts with NASA are in radiation engineering support for flight projects and research into the effects of radiation on complex electronic parts and systems.

Christina Seidleck has a bachelor's degree in computer science and has been performing a wide variety of application specific programming including user analysis, embedded as well as device driver codes within the radiation group for over 14 years.

Marty Carts received his BSEE at VPI&SU in 1984. Before working in the radiation effects field he served time in the broadcast radio equipment industry, the test and measurement equipment industry, and also in a small secure-communications research and development firm. Mr. Carts started work in the radiation effects field in 1993 at the Naval Research Laboratory in Washington, DC. In 1999 he moved to NASA Goddard Space Flight Center. His areas of specialty include high speed serial (both electrical and optical) communications, and complex tests.